REMARKS

An excess claim fee payment letter is submitted herewith for nine (9) additional total claims.

Claims 1-29 are all the claims presently pending in the application. Claims 1-10 are amended to more clearly define the invention and claims 11-29 are added. Claims 1, 6, and 11 are independent.

Applicant appreciates the courtesies extended to the Applicant's representative during a personal interview on February 9, 2005. During the personal interview, the Examiner agreed that the above-amendments to independent claims 1 and 6 overcome the applied references and agreed to further consider the language of independent claim 11 regarding the patterned area.

Support for new independent claim 11 may be found in the specification at, for example, page 9, line 8.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1-3, 5-8, and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Saito et al. reference in view of the Araki reference. Claims 4 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Saito et al. reference in view of the Araki reference and in further view of the Applicant's Admitted Prior Art.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention, as defined by, for example, independent claim 1, is directed to a method for fabricating a semiconductor device. The method includes depositing a metallic conductive film on an underlying insulating film, consecutively depositing first and second insulator films on the metallic conductive film, patterning the first and second insulator films to have a substantially same patterned area, etching the second insulator film selectively from the first insulator film to configure the second insulator film to have a bottom with a width smaller than a width of the first insulator film, patterning the metallic conductive film by using the first and second insulator films as an etching mask, depositing a third insulator film on the first and second insulator films and the underlying insulating film, etching-back the third insulator film to configure a side-wall film covering at least the patterned metallic conductive film, and depositing a fourth insulator film to embed therein the side-wall film on the underlying insulating film.

A second exemplary embodiment of the claimed invention, as defined by, for example, independent claim 11, is directed to a method for fabricating a semiconductor device. The method includes depositing a metallic conductive film on an underlying insulating film, depositing a first insulator film on the metallic conductive film, depositing a second insulator film on the first insulator film, patterning the first and second insulator films, etching the second insulator film to have a patterned area that is smaller than the first insulator film, and patterning the metallic conductive film.

Conventional methods for fabricating semiconductor devices have problems with defects such as a void and/or a short-circuit.

For example, in a first conventional method a two-layer mask is used to pattern a bit line. However, the use of a two-layer mask tends to increase the depth of sidewall films and, therefore, increases the aspect ratio between the depth of the sidewall films and the space between the sidewall films. This increased aspect ratio increases the likelihood that a defect, such as a void, is formed in an interlayer dielectric film. (Page 3, line 2 - 10).

In a second conventional method, a single-layer mask may be used to pattern a bit line. The use of a single-layer mask provides a reduced thickness in comparison to a two-layer mask and generally reduces the likelihood of forming a defect, such as a void, in an interlayer dielectric film. However, this reduction in thickness may result in an exposure of the bit lines when a contact hole is formed. This may result in a short-circuit defect. (Page 4, lines 3-23).

In summary, a two-layer hard mask may cause a defect in the embedding structure due to the increased aspect ratio, while a single-layer hard mask may cause a short circuit failure. (Page 5, lines 2-10).

In stark contrast, the present invention solves these problems by etching a second insulator film to have a patterned area (e.g., a bottom with a width) that is smaller than the first insulator film. In this manner, the present invention reduces the likelihood of a short circuit failure while enabling the use of a two-layer mask. (Page 6, lines 1 - 6).

II. THE PRIOR ART REJECTIONS

Regarding the rejection of claims 1-3, 5-8 and 10, the Office Action alleges that the Araki reference would have been combined with the Saito et al. reference to form the claimed invention and regarding the rejection of claims 4 and 9, the Office Action alleges that the

Applicant's Admitted Prior art would have been combined with the combination of the Araki and Saito et al. references to form the claimed invention

As agreed by Examiner Novacek during the personal interview, however, these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

As explained above, an exemplary embodiment of the present invention forms a cap layer using a two-layer hard mask 12, and 13 on a bit line 11. The upper insulator film 13 is etched using a wet-etching method (as recited by new dependent claims 27-29) to have a bottom with a width that is smaller than that of the lower insulator film 12 to improve the embedding efficiency of the insulation sidewall 16 between the bit lines 11.

In stark contrast, the Applicant's Admitted Prior Art teaches that the cap layer is made of a single-layer hard mask. The spattering method is used for selectively rounding the corners of the cap layer.

The wet-etching method cannot be used for the single cap layer. If the wet-etching method is used for the single cap layer, the top surface of the conductor layer is exposed.

In addition, using the single layer hard mask cannot provide enough margin to protect from short-circuit; therefore, the single hard mask should have a thickness enough to protect the conductor layer.

Further, the Saito et al. reference does not teach rounding the corners before disposing the sidewall.

The Saito et al. reference teaches a sidewall having a wide space between the adjoining gate electrodes for forming the lightly-doped drain structure, which does not require improvement of embedding efficiency.

Additionally, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different and unrelated matters and problems.

Specifically, the Saito et al. reference is directed to providing a technique for exposing semiconductor regions over the surface of a semiconductor substrate in self-alignment wiring lines which provides a lower aspect ratio for the connection holes and which prevents separation or bulging of a cap insulating film. (Col. 1, lines 8-11 and col. 3, lines 40-45).

In stark contrast, the Araki reference is concerned with the completely different and unrelated problem preventing deterioration of film coverage at the time of forming an interlayer film. (See: PROBLEM TO BE SOLVED).

One of ordinary skill in the art who was concerned with lowering aspect ratio for connection holes and preventing separation or bulging of a cap insulating film as the Saito et al. reference is concerned with addressing would not have referred to the Araki reference, and vice-versa, because the Araki reference is concerned with the completely different and unrelated problem of preventing deterioration of film coverage at the time of forming an interlayer film. Thus, the references would not have been combined.

Even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

As agreed by Examiner Novacek, none of the applied references teaches or suggests the features of the present invention including etching a second insulator film to configure the second insulator film to have a bottom with a width smaller than a width of the first insulator film as recited by independent claims 1 and 6. As explained above, this feature is important

for reducing the likelihood of a short circuit failure while enabling the use of a two-layer mask.

The Office Action admits that the Saito et al. reference does not teach or suggest this feature. The Office Action then attempts to rely upon the disclosure in the Araki reference to remedy the deficiencies of the Saito et. al. reference.

In particular, the Office Action alleges that the Araki reference "teaches that it is beneficial to etch the top (cap) layer on the metallic lines to narrow its width."

However, contrary to the Office Action's allegation, the Araki reference does not teach or suggest narrowing the width of the cap layer at all. Rather, the Araki reference discloses rounding the corners of the cap layer.

In particular, the Araki reference teaches that "the angle of said oxide film by which patterning was carried out, and (sic) is made round. . . . In case said oxide film is etched, the angle of an oxide film is dropped and it is made round." (Emphasis added, [0006]) "A part for the corner of the mask oxide film 105 upper part fails to be diminished by sputter etching, and etching section 105a with the round upper part is formed." (Emphasis added, [0012]). In other words, the Araki reference clearly discloses that the "angles" (i.e. upper corners) of the oxide film 105 is "diminished" (i.e. rounded) until the oxide film 105 has a "round upper part."

The Araki reference does not teach or suggest narrowing the width of the oxide film 105. Indeed, the width of the oxide film 105 clearly is not narrowed at all. Rather, only the upper corners or the oxide film 105 are rounded to form a round upper part.

Further, independent claims 1 and 6 require that the second insulator film has a bottom with a width smaller than a width of the first insulator film. In stark contrast, the

oxide layer 105 (or 105a) is clearly the same width as the underlying layers, such as the anti-reflection film 104, the aluminum alloy layer 103, etc.

Indeed, the Araki reference does not disclose any layer having a smaller width, let alone a second insulating layer having a smaller width than a first insulating layer.

Further, with respect to new independent claim 11, none of the applied references teaches or suggests the features of etching a second insulator film to have a patterned area that is smaller than the first insulator film.

As explained above, the Araki reference merely discloses rounding the upper corners of an oxide film 105 to form a round upper part. The Araki reference does not teach or suggest anything at all about etching the oxide film 105 to reduce the patterned area, let alone to reduce the patterned area so that it is smaller than another insulator film.

Therefore, the Examiner is respectfully requested to withdraw the rejections of claims 1-10.

III. FORMAL MATTERS AND CONCLUSION

The Office Action objects to the specification. In particular, the Office Alleges that the specification fails to provide proper antecedent basis for the first and second insulator films of "silicon nitride" and "silicon oxide" and that "the specification states that the first insulator is a "nitride" (not a *silicon* nitride) and the second insulator film is an "oxide" (not a *silicon* oxide)."

While Applicant submits that such would be clear to one of ordinary skill in the art to allow them to know the metes and bounds of the invention, taking the present Application as a whole, to speed prosecution claims 4 and 9 have been amended in accordance with

Examiner Novacek's very helpful suggestions.

In view of the foregoing, the Examiner is respectfully requested to withdraw this objection.

The Office Action also objects to claims 1 and 6 as allegedly being substantial duplicates.

However, as agreed by Examiner Novacek during the personal interview, while there are similarities in the language of claims 1 and 6, these claims are not substantial duplicates. Claim 1 is directed to a first exemplary embodiment of the present invention such as is, for example, described in the specification at, for example, page 8, line 10 - page 11, line 8 and claim 6 is directed to a second exemplary embodiment of the present invention such as is, for example, described in the specification at, for example, page 11, line 9 to page 13, line 6.

A difference between these two exemplary embodiments is that claim 1 recites consecutive (see preamble) steps of etching the second insulator film before patterning the metallic conductive film, while claim 6 recites consecutive (see preamble) steps of etching the second insulator film after patterning the metallic conductive film.

Therefore, contrary to the Examiner's allegation, claims 1 and 6 are not duplicates.

Further, in this regard, Applicant has added new independent claim 11, which recites etching the second insulator film and patterning the metallic conductive film without indicating the order/sequence. Rather, only claims 13 and 14 indicate any order at all between these features of the claimed method.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-29, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully

requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 2/23/05

James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254